CLAIMS

1. A method for reducing latency in conversions from a Serial Media Independent Interface (SMII) to a Media Independent Interface (MII), comprising:

generating receive and transmit clock signals from a physical layer device;

generating receive and transmit clock signals at a media access controller;

synchronizing the clock signals at the media access controller and the clock signals at the physical layer device such that MII clocks are generated from the SMII and a synchronization signal of the SMII is always delayed 8 nsec from a positive edge of the MII clock.

2. The method of claim 1 wherein the SMII is configured to receive digital information at the same time that the MII receives other digital information.

3. The method of claim 2 wherein the digital information is a nibble.

4. The method of claim 2 wherein the digital information is exchanged during a second part of a frame of the MII.

5. A SMII (Serial Media Independent Interface) to MII (Media Independent Interface) converter comprising:

an SMII that sends and receives frames that are configured to transmit data in an SMII standard format;

an MII that sends and receives frames that are configured to transmit data in an MII standard format;

an MII frame having a first part and a second part;

a first nibble being driven to the SMII at the second part of an MII frame;

a second nibble being received on the MII frame at the same time the first nibble is being driven to the SMII;

the MII having clocks that are generated from the SMII clock and synchronized such that latencies are reduced between conversions from SMII to MII.

6. The SMII to MII converter of claim 5 a synchronization signal of the SMII is always delayed 8 nsec from a positive edge of the MII clock.

7. A method for using standard FIFO techniques and a parallel to serial converter to convert nibble wide data to bit wide data in a data stream, the method comprising:

transmitting SMII frames such that frames are sent and received that are configured in an SMII standard format;

transmitting MII frames such that frames are sent and received that are configured in an MII standard format, the MII frames each having a first part and a second part;

driving a first nibble to the SMII at the second part of an MII frame;

receiving a second nibble on the MII at the same time the first nibble is being driven to the SMII;

generating MII clocks from an SMII clock; and

synchronizing the MII clock and the SMII clock such that latencies are reduced between conversions from SMII to MII.

8. The method of claim 7 wherein said synchronizing the MII clock and the SMII clock consistently delays a synchronization signal by 8 nsec from a positive edge of the MII clock.